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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,103	10/23/2003	Suzanne Mary Vining	TI-36373	6562

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,103	VINING, SUZANNE MARY	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-22** are presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 10/23/06 have been considered by the examiner (see attached PTO-1449).

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim objections

4. Claims 8 and 16, are objected to because of the following informalities:

Claim 8 recites, the phrase "that have" instead of "that has" (see line 4).

Claim 16 recites, the phrase "to be set" instead of "to set" (see line 4).

Claim 16 recites, the phrase "the toggle bit" instead of "a toggle bit" (see line 1).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U. S. C 112

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims **1, 7, 8, 10, 16 and 22** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Claim 1, recites the limitation "the data toggle phase" in line 11. There is insufficient antecedent basis for this limitation in the claim.

b) Referring to claim 1 line 9, there is insufficient antecedent basis for this limitation "the final recovered clock." Here it is understood that the applicant intended to claim "a final recovered clock".

c) As per claim 1, line 8 "**was possibly**" is indefinite and a positive term should be used.

d) Claim 7 recites "the block possibly-selected clock phase" which is inconsistent with what was previously recited (i.e. "the blocking component"): therefore, the recitation lack an antecedent basis.

e) Regarding claim 8 the phrase, "frequency of **about** the frequency" (see line 5) renders the claim indefinite. The examiner would appreciate if the applicant would clarify this matter.

f) Claim 10, recites the phrase "**substantially** evenly spaced". The claim is omnibus claim.

g) As per claim 16, line 1 the phrase "jitter **can** cause" is indefinite and a positive term should be used.

h) As per claim 22 line 3 "but **can be** some" is indefinite and a positive term should be used.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim **1-7 and 14-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maddux (hereinafter referred to as "Maddux") (US 6,529,148) in view of Millar (U.S. PN: 6,337,590).

As per claims 1, 14 and 18:

Maddux substantially discloses (Fig. 1. element 150) a data recovery device (col. 1, lines 7-9) comprising a number of sample components (block 230 of Fig. 2) that obtain (or generate) samples (d1 ...dN) of a received serial data stream (115) at a number of phases (231), wherein the number of phases are successively offset (column 3, lines 37-41) throughout a bit time period and the samples are obtained throughout the time period at the number of phases (N different phases; a number of transition

detectors (Maddux uses the term "edge detector", block 250 of Fig. 2) corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions (column 3, lines 45-*, and a first circuit (including logic blocks 240 and/or 280 as compared to the OR gate 508 of the inventive Fig. 5A) that generates a serial decoded data stream (recovered data) that comprises values for time periods) according to occurrence or non occurrence of one or more transitions within the respective time periods. Maddux **does not explicitly** teach a blocking component for blocking clock phase and selecting a clock phase according to a data toggle phase. **However**, Millar teaches a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been established and the jitter filter has been enabled by the output of flip-flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9). **Therefore,** it would have been obvious to one person having ordinary skills in the art at the time the invention was made to implement or incorporate the teaching Miller's toggling operation for blocking a clock phases into the invention of Maddux to provide efficient and reliable operation. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to achieve a significant tolerance to system clock jitter with reliable start-up locking (see col. 3, lines 49-51).

As per claim 2:

Maddux in view of Miller teach all the subject matter claimed in claim 1 including Millar teaches a digital delay locked loop circuit is shown which includes a phase detector 25 comprised of a single D-type flip-flop, which compares the reference (system) clock signal CLKR, applied to the CLK input of flip-flop 25, with the internal fed back clock signal CLKI, applied to the D input of flip-flop 25 (see col. 6, last paragraph).

As per claims 3 and 4:

Maddux discloses an oversampler (230) conducts samples over a time period for the data bit signal, based on the "N" clock signals 231 provided to the oversampler. Each of these "N" clock signals (231) is at different phases so that data is sampled at a rate faster than the data rate. The resultant "N" data samples (d.sub.1 -d.sub.N) (235) are provided to data pipeline logic (240), which provides sufficient delay to enable proper analysis of the data samples 235 (see column 3, lines 25-45).

As per claim 5:

Maddux discloses one technique for edge location detection involves the Exclusive OR'ing (XOR'ing) of adjacent data samples where data sample is separately XORed with data sample, and data sample. For instance, data sample d.sub.1 is XOR'ed with data sample d.sub.2 (d.sub.1.sym.d.sub.2) and data sample d.sub.N (d.sub.1.sym.d.sub.N). Data sample d.sub.3 is XOR'ed with data sample d.sub.2 (d.sub.3.sym.d.sub.2) and data d.sub.4 (d.sub.3.sym.d.sub.4). When the edge detector logic 250 computes the XOR results for both adjacent data sample (d.sub.i.sym.d.sub.i-

1) and (d.sub.i.sym.d.sub.i+1) and such results are equal to "1", it has detected an apparent edge of the data bit signal at a location associated with data sample d.sub.i. (see col. 3, lines 49-63).

As per claim 6:

Maddux in view Millar teach all the subject matter claimed in clam 1 including Millar teaches Miller teaches a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been established and the jitter filter has been enabled by the output of flip-flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9).

As per claims 7:

The claim is rejected under similar rationale as set forth in claim 1.

As per claims 15-17:

Maddux in view of Millar teach all the subject matter claimed in claim 14 including Millar a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been established and the jitter filter has been enabled by the output of flip-flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS

pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9).

As per claims 19:

Maddux discloses generating a number of phase clocks (N phases) successively offset throughout the time period (column 3, lines 37-41).

As per claims 20:

Maddux discloses one technique for edge location detection involves the Exclusive OR'ing (XOR'ing) of adjacent data samples where data sample is separately XORed with data sample, and data sample. For instance, data sample d.sub.1 is XOR'ed with data sample d.sub.2 (d.sub.1.sym.d.sub.2) and data sample d.sub.N (d.sub.1.sym.d.sub.N). Data sample d.sub.3 is XOR'ed with data sample d.sub.2 (d.sub.3.sym.d.sub.2) and data d.sub.4 (d.sub.3.sym.d.sub.4). When the edge detector logic 250 computes the XOR results for both adjacent data sample (d.sub.i.sym.d.sub.i-1) and (d.sub.i.sym.d.sub.i+1) and such results are equal to "1", it has detected an apparent edge of the data bit signal at a location associated with data sample d.sub.i. (see col. 3, lines 49-63).

As per claim 21-22:

Maddux in view of Millar teach all the subject matter claimed in claim 14 including Millar a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been

established and the jitter filter has been enabled by the output of flip-flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9).

7. Claims **8-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maddux (hereinafter referred to as "Maddux") (US 6,529,148) in view of Mukherjee et al. (U.S. PM: 6,760389).

As per claim 8:

Maddux discloses (Fig. 1. element 150) a data recovery device (col. 1, lines 7-9) comprising a number of sample components (block 230 of Fig. 2) that obtain (or generate) samples (d1 ...dN) of a received serial data stream (115) at a number of phases (231), wherein the number of phases are successively offset (column 3, lines 37-41) throughout a bit time period and the samples are obtained throughout the time period at the number of phases (N different phases; a number of transition detectors (Maddux uses the term "edge detector", block 250 of Fig. 2) corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions (column 3, lines 45-*, and a first circuit (including logic blocks 240 and/or 280 as compared to the OR gate 508 of the inventive Fig. 5A) that generates a serial decoded data stream (recovered data) that comprises values for time periods) according to occurrence or non occurrence of one or more transitions within the respective time periods. Maddux **does not explicitly** teach a select clock for selecting a

clock phase and generates a selected clock. **However**, Mukherjee et al. in an analogous art, in figure 2 teach a data and clock recovery circuit (130), a poly-phase edge generator or n-phase clock synthesizer (200) is connected to the destination clock (145) and outputs n-equally spaced clock edges/cycles (or sampling signals) to a sampling circuit (202). The sampling circuit also receives the data stream (125) and includes a multiple transition detector (205) the outputs of which are coupled to an edge counter and sum accumulator 210. Based on this binary number, the decision circuit (215) outputs a "phase select" signal to a clock select circuit (217), the output of which is the recovered clock signal on line (140). In response to the "phase select" signal, the clock select circuit (217) selects one of the clock edges and outputs the selected clock edge as a recovered clock signal to a data decoder (220) so that data recovery is performed (see col. 4, last paragraph and col. 5, lines 1-16). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made incorporate the teachings of Maddux using a "phase select" signal to a clock select circuit (217), the output of which is the recovered clock signal on line 140 and in response to the "phase select" signal, the clock select circuit 217 selects one of the clock edges and outputs the selected clock edge as a recovered clock signal to a data decoder 220 so that data recovery is performed as taught by Mukherjee et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to achieve a clock/data recovery or PLL with a reduced sensitivity that meets the needs of the tracking the clock frequency of a network (see col. 3, lines 1-4).

As per claims 9-13:

Maddux discloses a data recovery component (150) that identifies transitions (this is done by the edge detector 250) in the received serial data stream (115) and obtains a recovered serial data stream (recovered data output of the mux (280)) based solely on the identified transitions (see col. 3, lines 49-53).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,671,258 Burns et al.

US PN: 6,981,168 Schmatz et al.

US PN: 5,276,712 Pearson, Jonathan

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status

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Esaw Abraham

Art unit: 2133

GUY LAMARRE
PRIMARY EXAMINER